AMENDMENTS TO CLAIMS

Kindly amend claims 1-7 and cancel claims 8-16 as follows.

1. (Currently Amended) A freeway routing system for a field programmable gate array ~~(FPGA)~~, the FPGA comprising a plurality of tiles, each tile having a plurality of functional groups arranged in rows and columns, a plurality of interface groups surrounding said plurality of functional groups such that one interface group is positioned at each end of each row and column, each of the interface groups having input ports and output ports, said freeway system comprising:

~~a plurality of FPGA tiles, each FPGA tile comprising:~~

~~a plurality of functional groups (FGs) arranged in rows and columns;~~

~~a plurality of interface groups (IGs) surrounding said plurality of FGs such that one IG is positioned at each end of each row and column, each of the IGs having a first, second and third set of input ports and a first, second and third set of output ports;~~

a first ~~freeway~~ set of routing conductors configured to transfer signals to the ~~first, second and third~~ input ports of ~~IGs~~ at least one interface group in ~~one FPGA~~ a first one of said plurality of tiles and configured to transfer signals from ~~said first, second and third~~ the output ports of the ~~IGs of all other FPGA tiles~~ interface groups in the remainder of the plurality of tiles;

said ~~freeway~~ first set of routing conductors comprising:

a plurality of vertical conductors that form intersections with a plurality of horizontal conductors; and

programmable interconnect elements located at said intersections ~~in a diagonal orientation on said FPGA tile~~ of said plurality of vertical conductors and said plurality of horizontal conductors in a diagonal orientation thus connecting each one of said plurality of horizontal conductors to one of said plurality of vertical conductors.

2. (Currently Amended) The ~~FPGA~~ freeway system of Claim 1~~, wherein said FPGA~~ further ~~comprises~~ comprising:

~~at least one other FPGA tile configured in the same manner as said first FPGA;~~

~~wherein the freeway set of routing conductors of each FPGA tile are connected to any adjacent FPGA tile's freeway set of routing conductors.~~

a second set of routing conductors configured to transfer signals to the input ports of at least one interface group in a second one of said plurality of tiles adjacent to said first one of said plurality of tiles and configured to transfer signals from the output ports of the interface groups in the remainder of the plurality of tiles wherein said second set of conductors connect to said first set of conductors;

said second set of routing conductors comprising:

a plurality of vertical conductors that form intersections with a plurality of horizontal conductors; and

programmable interconnect elements located at said intersections of said plurality of vertical conductors and said plurality of horizontal conductors in a diagonal orientation thus connecting each one of said plurality of horizontal conductors to one of said plurality of vertical conductors.

3. (Currently Amended) The ~~FPGA~~ freeway system of Claim 2, wherein ~~said FPGA further comprises~~:

the programmable interconnect elements located at connections between adjacent ~~FPGA tiles~~ the first and the second sets of conductors.

4. (Currently Amended) The ~~FPGA~~ system of Claim 1, wherein said diagonally oriented programmable interconnects are arranged from the upper left corner of said first ~~FPGA~~ one of said plurality of ~~tile~~ tiles to the lower right corner of said first ~~FPGA tile~~ one of said plurality of tiles.

5. (Currently Amended) The ~~FPGA~~ system of Claim 1, wherein said diagonally oriented programmable interconnects are arranged from the upper right corner of said first ~~FPGA~~ one of said plurality of ~~tile~~ tiles to the lower left corner of said first ~~FPGA tile~~ one of said plurality of tiles.

6. (Currently Amended) The ~~FPGA~~ system of Claim 1, wherein said ~~freeway~~ first set of routing conductors are further configured to also transfer signals from the output ports of at least one ~~IO~~ Input/Output.

7. (Currently Amended) The ~~FPGA~~ system of Claim 1, wherein said ~~freeway~~ first set of routing conductors are further configured to also transfer signals from the output ports of at least one RAM.

8. (Cancelled) A method of routing the internal components in a FPGA tile comprising:

inputting a function netlist defining a user circuit;

optimizing said user circuit;

placing user cells defining said user circuit into said FPGA internal components;

using a first set of routing conductors to route said user circuit to interconnect said internal components to implement said user circuit; and

engaging a freeway set of routing conductors to meet said user circuit routing requirements;

generating a programming bitstream defining said user circuit; and

programming said FPGA functional unit with said bitstream to implement said user circuit.

9. (Cancelled) A method of routing the internal components in a FPGA tile comprising:

inputting a function netlist defining a user circuit;

optimizing said user circuit;

placing user cells defining said user circuit into said FPGA internal components;

using a first set of routing conductors and a freeway set of routing conductors to route said user circuit to interconnect said internal components to implement said user circuit;

generating a programming bitstream defining said user circuit; and

programming said FPGA functional unit with said bitstream to implement said user circuit.

10. (Cancelled) A method of providing a freeway interconnect structure in a FPGA comprising:

providing a plurality of FPGA tiles;

providing a plurality of functional groups (FGs) arranged in rows and columns on each said FPGA tile;

providing a plurality of interface groups (IGs) surrounding said plurality of FGs such that one IG is positioned at each end of each row and column, each of the IGs having a first, second and third set of input ports and a first, second and third set of output ports;

providing a freeway set of routing conductors configured to transfer signals to said first, second and third input ports of IGs of one FPGA tile, and configured to transfer signals from said first, second and third output ports of IGs of all other FPGA tiles;

said act of providing a freeway set of routing conductors comprising:

providing a plurality of vertical conductors that form intersections with a plurality of horizontal conductors; and

providing programmable interconnect elements located at said intersections in a diagonal orientation on said FPGA tile.

11. (Cancelled) The method of Claim 10 further comprising:

providing at least one other FPGA tile configured in the same manner as said first FPGA; and

connecting said freeway set of routing conductors of each FPGA tile to any adjacent FPGA tile's freeway set of routing conductors.

12. (Cancelled) The method of Claim 11, further comprising:

providing programmable interconnect elements located at said connections between adjacent FPGA tiles.

13. (Cancelled) The method of Claim 10, further comprising configuring said freeway set of routing conductors to also transfer signals from output ports of at least one IO.

14. (Cancelled) The method of Claim 10, further comprising configuring said freeway set of routing conductors to also transfer signals from output ports of at least one RAM.

15. (Cancelled) An apparatus for routing the internal components in a FPGA tile comprising:

means for inputting a function netlist defining a user circuit;

means for optimizing said user circuit;

means for placing user cells defining said user circuit into said FPGA internal components;

means for using a first set of routing conductors to route said user circuit to interconnect said internal components to implement said user circuit;

means for determining whether the routing requirements of said user circuit have been met using said first set of routing conductors;

means for engaging a freeway set of routing conductors to meet said user circuit routing requirements;

means for generating a programming bitstream defining said user circuit; and

means for programming said FPGA functional unit with said bitstream to implement said user circuit.

16. (Cancelled) An apparatus for routing the internal components in a FPGA tile comprising:

means for inputting a function netlist defining a user circuit;

means for optimizing said user circuit;

means for placing user cells defining said user circuit into said FPGA internal components;

means for using a first set of routing conductors and a freeway set of routing conductors to route said user circuit to interconnect said internal components to implement said user circuit;

means for generating a programming bitstream defining said user circuit; and

means for programming said FPGA functional unit with said bitstream to implement said user circuit.